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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,904	12/28/2001	Juan G. Revilla	10559-567001/P12729	8892
20985	7590	07/28/2004		
FISH & RICHARDSON, PC 12390 EL CAMINO REAL SAN DIEGO, CA 92130-2081			EXAMINER VO, TIM T	
			ART UNIT 2112	PAPER NUMBER

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/040,904	REVILLA ET AL.	
	Examiner	Art Unit	
	Tim T. Vo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 28 December 2001.  
 2a) This action is FINAL.                            2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-32 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-8, 10-22 and 24-32 is/are rejected.  
 7) Claim(s) 9 and 23 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 28 December 2001 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date 7/23/04.

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application (PTO-152)  
 6) Other: \_\_\_\_\_.

## Part III DETAILED ACTION

### ***Notice to Applicant(s)***

This application has been examined. Claims 1-32 are pending.

### ***Drawings***

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the bridge must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-8, 10-22 and 24-32 are rejected under 35 U.S.C. § 102(e) as being anticipated by Wakimoto et al. EP 1,103,898 referred hereinafter "Wakimoto".

As for claims 1, 15, 30 and 32, Wakimoto teaches a method comprising routing a memory access from a processor core back into the processor core through a bus interface coupled to the processor core (see figure 1, processor core 11 accessing local memory 3, main memory 2 via the bus interface 13).

As for claims 2-3 and 16-17, Wakimoto teaches determining a status of a re-routing bridge in the bus interface (see figure 1, bus bridge 5, bus interface 13, wherein the bus bridge 5 routes data from the main memory 2 to the bus interface 13 then into the processor core 11);

determining an address of the memory to be accessed (see figure 2, memory management units 62-63 locates within the processor core managing addresses to be accessed from the local memory 3 and main memory 2); and

placing the access on a bus back into the processor core in response to the bridge being enabled and the address being in a local memory address space (see

figure 1-3, disclose the memory management units 62-63 determining logical address and physical address for accessing data from the main memory 2 and local memory 3 via the bridge 5 and bus interface 13).

As for claims 4-6, 18-20 and 31, Wakimoto teaches accessing local memory, SRAM (see figure 1, local memory 3, SRAM column 1 lines 26-31).

As for claims 7 and 21, Wakimoto teaches routing a memory access from the processor core comprises routing a memory access from a digital signal processor core (see figures 1-2, CPU 6).

As for claim 8, Wakimoto teaches a processor core including a memory including a local data memory and a local instruction memory (see figure 1, local memory 3, instruction cache 12),

a first port coupled to the local data memory (see figure 1, bus 43), and a second port coupled to the local data memory and the local instruction memory (see figure 1, bus 41);

a bus interface including a first bus coupled to the first port (see figure 1, bus 43),

a second bus coupled to the second port (see figure 1, bus 41),

a bridge between the first bus and the second bus (see figure 1, bus interface 13), and a multiplexing unit operative to switch between the second bus and the bridge to enable information placed onto the first bus to be routed into the second port (see figure 1, interface unit routing data from local memory 3, main memory 2).

As for claims 10, 29, Wakimoto teaches the local memory comprises a Level 1 SRAM (see column 1 lines 26-31).

As for claims 11-12, Wakimoto teaches the first port comprises a fill port and the first port comprises a fill bus (see figure 1, bus 43, 41).

As for claims 13-14, Wakimoto teaches the processor core further comprises an interface coupled to the second port, the interface being operable to access the local data memory and local instruction memory (see figure 1, bus 41, 43, local memory 3, instruction cache 12).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 22 and 24-28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wakimoto.

As for claim 22, Wakimoto teaches a processor core including a memory including a local data memory and a local instruction memory (see figure 1, local memory 3, instruction cache 12),

a first port coupled to the local data memory (see figure 1, bus 43), and a second port coupled to the local data memory and the local instruction memory (see figure 1, bus 41);

a bus interface including a first bus coupled to the first port (see figure 1, bus 43), a second bus coupled to the second port (see figure 1, bus 41),

a bridge between the first bus and the second bus (see figure 1, bus interface 13), and a multiplexing unit operative to switch between the second bus and the bridge to enable information placed onto the first bus to be routed into the second port (see figure 1, interface unit routing data from local memory 3, main memory 2).

Wakimoto does not expressly teach USB bus interface. "Official Notice" is taken that both concept and the advantages for utilizing USB in the computer system such as Wakimoto's system are well known and expected in the art. It would have been obvious to include the USB to Wakimoto because it providing system expansion up to 127 peripherals and also supports hot plugging.

As for claims 24, Wakimoto teaches the local memory comprises a Level 1 SRAM (see column 1 lines 26-31).

As for claims 25-26, Wakimoto teaches the first port comprises a fill port and the first port comprises a fill bus (see figure 1, bus 43, 41).

As for claims 27-28, Wakimoto teaches the processor core further comprises an interface coupled to the second port, the interface being operable to access the local data memory and local instruction memory (see figure 1, bus 41, 43, local memory 3, instruction cache 12).

### ***Allowable Subject Matter***

4. Claims 9 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tim T. Vo  
Primary Examiner  
Art Unit 2112

7/23/04